Claims

1. A material composition comprising elements of Si, C, O and H, said composition having a covalently bonded structure and a dielectric constant of not more than 3.6.

2. A material composition according to claim 1, wherein said composition further comprises between about 5 and about 40 atomic percent of Si; between about 5 and about 45 atomic percent of C; between 0 and about 50 atomic percent of O; and between about 10 and about 55 atomic percent of H.

3. A material composition according to claim 1, wherein said composition having a covalently bonded three-dimensional network.

4. A material composition according to claim 1, wherein said composition having a covalently bonded ring network.

5. A material composition according to claim 1, wherein said composition being thermally stable to a temperature of at least 350°C.

6. A film formed of the material composition according to claim 1, wherein said film having a thickness of not more than 1.3 micrometers and a crack propagation velocity in water of less than 10^{-9} m/s.

7. A film according to claim 6, wherein said crack propagation velocity in water is less than 10^{-10} m/s.

8. A material composition according to claim 1, wherein said Si atoms are at least partially submitted by Ge atoms.

9. A material composition according to claim 1, wherein said composition preferably having a covalently bonded ring network and a dielectric constant of not more than 3.2.

10. A material composition according to claim 1 further comprising at least one element selected from the group consisting of F, N, and Ge.

11. A method for fabricating a thermally stable low dielectric constant film comprising the steps of:

providing a plasma enhanced chemical vapor deposition (PECVD) chamber,

positioning substrate in said chamber,

flowing a precursor gas containing Si and at least two elements selected from the group consisting of C, O and H into said PECVD chamber, and

depositing a hydrogenated silicon carbon or hydrogenated oxidized silicon carbon film on said substrate.

12. A method according to claim 11, wherein said plasma enhanced chemical vapor deposition chamber is a parallel plate type plasma reactor.

13. A method according to claim 11, wherein a plasma in said PECVD is run in a continuous mode during film deposition.

14. A method according to claim 11, wherein a plasma in said PECVD is run in a pulsed mode during film deposition.

15. A method according to claim 11 further comprising the step of flowing a precursor gas comprising molecules of a ring structure into said PECVD chamber.

16. A method according to claim 11 further comprising the step of selecting a precursor having molecules with ring structures from the group consisting of 1,3,5,7-tetramethylcyclotetrasiloxane (TMCTS, or $C_4H_{16}O_4Si_4$), tetraethylcyclotetrasiloxane ($C_8H_{24}O_4Si_4$), decamethylcyclopentasiloxane ($C_{10}H_{30}O_5Si_5$), and precursor mixtures comprising Si, O, and C.

17. A method according to claim 15, wherein said precursor gas is TMCTS.

18. A method according to claim 11 further comprising the step of mixing said precursor with at least one member selected from the group consisting of hydrogen, oxygen, germanium, nitrogen or fluorine containing gases.

19. A method for fabricating a thermally stable hydrogenated oxidized silicon carbon low dielectric constant film according to claim 11 further comprising optionally the step of heat treating said film at a temperature not higher than 300°C for a first time period and heat treating said film at a temperature not lower than 300°C for a second time period, said second time period being longer than said first time period.

20. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure comprising:

a pre-processed semiconducting substrate having a first region of metal embedded in a first layer of insulating material,

a first region of conductor embedded in a second layer of insulating material which comprises SiCOH, said second layer of insulating material being in intimate contact with said first layer of insulating material, said first region of conductor being in electrical communication with said first region of metal, and

a second region of conductor being in electrical communication with said first region of conductor and being embedded in a third layer of insulating material comprising SiCOH, said third layer of insulating material being in intimate contact with said second layer of insulating

material.

21. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure according to claim 20 further comprising a dielectric cap layer situated in-between said second layer of insulating material and said third layer of insulating material.

22. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure according to claim 20 further comprising:

a first dielectric cap layer between said second layer of insulating material and said third layer of insulating material, and

a second dielectric cap layer on top of said third layer of insulating material.

23. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure according to claim 21, wherein said dielectric cap layer being formed of a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxinitride, refractory metal silicon nitride with the refractory metal being Ta, Zr, Hf or W, silicon carbide, silicon carbo-oxide, their hydrogen-containing compounds and modified SiCOH.

24. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure according to claim 22, wherein said first and said second

dielectric cap layers are formed of a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxinitride, refractory metal silicon nitride with the refractory metal being Ta, Zr, Hf or W, silicon carbo-oxide, their hydrogen-containing compounds and modified SiCOH.

25. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure according to claim 20, wherein said first layer of insulating material is silicon oxide, silicon nitride, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG) or other doped varieties of these materials.

26. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure according to claim 20 further comprising:

a diffusion barrier layer of a dielectric material deposited on at least one of said second layer of insulating material and said third layer of insulating material.

27. An electronic structure having layers of insulating material as an intralevel or interlevel dielectrics in a wiring structure according to claim 20 further comprising:

a dielectric reactive ion etching (RIE) hard mask/polish stop layer on top of said second layer of insulating material, and

a dielectric diffusion barrier layer on top of said RIE hard mask/polish stop layer.

28. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure according to claim 20 further comprising:

a first dielectric RIE hard mask/polish stop layer on top of said second layer of insulating material,

a first dielectric diffusion barrier layer on top of said first dielectric RIE hard mask/polish stop layer,

a second dielectric RIE hard mask/polish stop layer on top of said third layer of insulating material, and

a second dielectric diffusion barrier layer on top of said second dielectric RIE hard mask/polish stop layer.

29. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure according to claim 28 further comprising a dielectric cap layer between an interlevel dielectric of SiCOH and an intralevel dielectric of SiCOH.

30. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure comprising:

a pre-processed semiconducting substrate having a first region of metal embedded in a first layer of insulating material, and

at least one first region of conductor embedded in at least one second layer of insulating material which comprises SiCOH, one of said at least one second layer of insulating

material being in intimate contact with said first layer of insulating material, one of said at least one first region of conductor being in electrical communication with said first region of metal.

31. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure according to claim 30 further comprising a dielectric cap layer situated in-between each of said at least one second layer of insulating material.

32. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure according to claim 30 further comprising:

a first dielectric cap layer between each of said at least one second layer of insulating material, and

a second dielectric cap layer on top of said topmost second layer of insulating material.

33. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure according to claim 32, wherein said first and said second dielectric cap layers are formed of SiCOH or modified SiCOH.

34. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure according to claim 31, wherein said dielectric cap layer being formed of a selected material selected from the group consisting of silicon oxide, silicon

nitride, silicon oxinitride, refractory metal silicon nitride with the refractory metal being Ta, Zr, Hf or W, silicon carbide, silicon carbo-oxide, their hydrogen-containing compounds and modified SiCOH.

35. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure comprising:

a pre-processed semiconducting substrate having a first region of metal embedded in a first layer of insulating material,

a first region of conductor embedded in a second layer of insulating material, said second layer of insulating material being in intimate contact with said first layer of insulating material, said first region of conductor being in electrical communication with said first region of metal,

a second region of conductor being in electrical communication with said first region of conductor and being embedded in a third layer of insulating material, said third layer of insulating material being in intimate contact with said second layer of insulating material,

a first dielectric cap layer between said second layer of insulating material and said third layer of insulating material, and

a second dielectric cap layer on top of said third layer of insulating material wherein said first and said second dielectric cap layers are formed of a material comprising atoms of Si, C, O and H.

36. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure comprising:

a pre-processed semiconducting substrate having a first region of metal embedded in a first layer of insulating material,

a first region of conductor embedded in a second layer of insulating material, said second layer of insulating material being in intimate contact with said first layer of insulating material, said first region of conductor being in electrical communication with said first region of metal,

a second region of conductor being in electrical communication with said first region of conductor and being embedded in a third layer of insulating material, said third layer of insulating material being in intimate contact with said second layer of insulating material, and

a diffusion barrier layer formed of a material comprising atoms of Si, C, O and H deposited on at least one of said second layer and said third layer of insulating material.

37. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure comprising:

a pre-processed semiconducting substrate having a first region of metal embedded in a first layer of insulating material,

a first region of conductor embedded in a second layer of insulating material, said second layer of insulating material being in intimate contact with said first layer of insulating material, said first region of conductor being in electrical communication with said first region of

metal,

a second region of conductor being in electrical communication with said first region of conductor and being embedded in a third layer of insulating material, said third layer of insulating material being in intimate contact with said second layer of insulating material,

a reactive ion etching (RIE) hard mask/polish stop layer on top of said second layer of insulating material, and

a diffusion barrier layer on top of said RIE hard mask/polish stop layer, wherein said RIE hard mask/polish stop layer and said diffusion barrier layer are formed of a material comprising atoms of Si, C, O and H.

38. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure comprising:

a pre-processed semiconducting substrate having a first region of metal embedded in a first layer of insulating material,

a first region of conductor embedded in a second layer of insulating material, said second layer of insulating material being in intimate contact with said first layer of insulating material, said first region of conductor being in electrical communication with said first region of metal,

a second region of conductor being in electrical communication with said first region of conductor and being embedded in a third layer of insulating material, said third layer of insulating material being in intimate contact with said second layer of insulating material,

a first RIE hard mask/polish stop layer on top of said second layer of insulating material,

a first diffusion barrier layer on top of said first RIE hard mask/polish stop layer,

a second RIE hard mask/polish stop layer on top of said third layer of insulating material, and

a second diffusion barrier layer on top of said second RIE hard mask/polish stop layer, wherein said RIE hard mask/polish stop layers and said diffusion barrier layers are formed of a material comprising atoms of Si, C, O and H.

39. An electronic structure having layers of insulating material as intralevel or interlevel dielectrics in a wiring structure according to claim 38 further comprising a dielectric cap layer formed of a material comprising Si, C, O and H situated between an interlevel dielectric layer and an intralevel dielectric layer.